CLAIMS

We Claim:

1. An input/output circuit for an integrated circuit comprising:

an input pad;

a follower circuit coupled to the input pad;

a pull-up circuit coupled to the input pad; and

a pull-down circuit coupled to the input pad.

2. A method for an input/output circuit for an integrated circuit comprising:

tri-stating an output buffer; and

providing one of a weak pull-up, a weak pull-down, and a pad signal follower on an input pad.

3. An input/output circuit for an integrated circuit comprising:

an input pad;

a pull-up circuit coupled to the input pad;

a first multiplexer having a control terminal receiving values from a first plurality of memory cells, the first multiplexer having a first output signal coupled to a control terminal of the pull-up circuit;

a pull-down circuit coupled to the input pad;

a second multiplexer having a control terminal receiving values from a second plurality of memory cells, the second multiplexer having a second output signal coupled to a control terminal of the pull-down circuit;

a tri-state buffer coupled to the input pad;

a third multiplexer having a control terminal receiving a value from a first memory cell at a first input terminal and receiving a first user-defined value at a second input terminal, the third multiplexer having a third output signal coupled to an enable terminal of the tri-state buffer; and

a fourth multiplexer having a control terminal receiving a value from a second memory cell at a first input terminal and receiving a second user-defined value at a second input terminal, the fourth multiplexer having a fourth output signal coupled to a data output terminal of the tri-state buffer;

wherein a configuration signal from a user-defined logic circuit is provided to the control terminals of the first, second, third, and fourth multiplexers.

4. A method for an input/output circuit for an integrated circuit comprising:

providing a pull-up circuit to an input pad of the input/output circuit;

using a configuration signal to select between a first plurality of memory cells, thereby controlling the pull-up circuit;

providing a pull-down circuit to an input pad of the input/output circuit;

using the configuration signal to select between a second plurality of memory cells, thereby controlling the pull-down circuit;

providing control signals to a tri-state buffer coupled to the input pad; and

using the configuration signal to select between a plurality of signals used to control define the control signals.

5. A method for providing a minimal hold time relative to a fixed global clock for the data provided to an input/output circuit of a programmable integrated circuit, the method comprising:

providing a fixed clock signal to the input/output circuit;

providing a data signal to the input/output circuit;

receiving the data signal with a programmable delay circuit; and

providing the delayed data signal to an input register.

6. The method of Claim 5 further including the step of controlling the amount of delay in the programmable delay circuit with values stored in memory cells.

7. A circuit for delaying a data input signal to an input/output circuit of an integrated circuit comprising:

a plurality of memory cells;

a delay structure having control inputs coupled to the plurality of memory cells;

a data input pad for receiving a data input signal coupled to a data input terminal of the delay structure;

a clock distribution system having a fixed delay;

a clock input pad for receiving a clock input signal coupled to an input terminal of the clock distribution system;

a multiplexer having a first input terminal coupled to an output terminal of the input delay system and having a second input terminal coupled to the data input pad;

a first memory cell coupled to a control terminal of the multiplexer; and

an input register having a data input terminal coupled to an output terminal of the multiplexer and having a clock input terminal coupled to an output terminal of the clock distribution system.

8. A circuit for delaying a data signal comprising:

a first inverter;

a second inverter coupled to an output terminal of the first inverter;

a first plurality of p-channel transistor pairs coupled between a first supply voltage and a first supply rail of the first inverter, one of each transistor pair having a gate coupled to a second supply voltage;

a first plurality of n-channel transistor pairs coupled between a third supply voltage and a second supply rail of the first inverter, one of each transistor pair having a gate coupled to a fourth supply voltage;

a first capacitor pair having a control terminal coupled to an output terminal of the second inverter;

a third inverter coupled to the control terminal of the first capacitor pair;

a second plurality of p-channel transistor pairs coupled between a fifth supply voltage and a first supply rail of the third inverter, one of each transistor pair having a gate coupled to a sixth supply voltage;

a first plurality of n-channel transistor pairs coupled between a seventh supply voltage and a second supply rail of the third inverter, one of each transistor pair having a gate coupled to a eighth supply voltage;

a second capacitor pair having a control terminal coupled to an output terminal of the third inverter; and

a fourth inverter coupled to an output terminal of the third inverter.

9. A method for delaying a data signal comprising:

providing a data signal to a delay circuit;

buffering the data signal;

inverting the data signal with an inverter having supply rails supplied by series resistor circuits;

passing the data signal through a capacitor pair;

inverting the data signal with an inverter having supply rails supplied by series resistor circuits;

passing the data signal through a capacitor pair; and

buffering the data signal.

10. A circuit for testing an input/output circuit comprising:

a multiplexer coupled to a horizontal bus;

a multiplexer coupled to a vertical bus;

an OR gate having a first input terminal coupled to the first multiplexer and a second input terminal coupled to the second multiplexer;

wherein the output terminal of the OR gate is coupled to an input of the input/output circuit.

11. A method of testing an input/output circuit, the method comprising:

providing a first signal from a horizontal bus;

providing a second signal from a vertical bus;

coupling the first and second signals into a third signal; and

providing the third signal to an input of the input/output circuit.

12. A circuit for transferring data from a first data input pad to a second data input pad comprising:

a transistor; and

a buffer having an output terminal coupled to the transistor, having a first source/drain region coupled to the first data input pad, and having a second source/drain region coupled to the second data input pad;

wherein a control signal provided from the buffer to the transistor either couples or de-couples the first and second input pads.

13. A method for transferring data from a first data input pad to a second data input pad, the method comprising providing a control signal to a first transistor switch, thereby coupling or de-coupling the first and second input pads.

14. A method of increasing the number of channels available for a direct input/output connection to an input/output circuit for an integrated circuit comprising:

providing a bypass signal to a first input terminal of an OR gate;

providing an output enable signal to a second input terminal of the OR gate;

providing an output signal of the OR gate to a gate of a transistor;

providing an input data signal to a source of the transistor;

providing the signal at a drain of the transistor to a storage latch;

providing an output signal of the storage latch to a first route of a routing structure; and

providing the input data signal to a second route of the routing structure.

15. An edge-placed I/O tile structure comprising:

an OR gate;

a horizontal channel multiplexer coupled to a first input terminal of the OR gate;

a vertical channel multiplexer coupled to a second input terminal of the OR gate; and

an I/O circuit coupled to an output terminal of the OR gate.

16. The edge-placed tile structure of Claim 14 further comprising a second identical edge-placed tile structure.